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Coherent MM Wave Radar Using Incoherent Transmitter

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13. ABSTRACT *(Maximum 200 words)*

A coherent MM wave radar using an incoherent transmitter is described. A breadboard of such a radar was constructed and successfully tested.

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CONTENTS

COHERENT MM WAVE RADAR USING INCOHERENT TRANSMITTER

0. Summary

A breadboard of a coherent mm wave radar using an incoherent transmitter was designed and tested. As transmitter was used an Extended Interaction Oscillator operating at 94 GHz with 1 kW pulse output power. The pulse peak to clutter ratio behind the synchronous detector was measured to be 26 dB for single pulse. It appears that this ratio was limited by phase noise performance in the receiver local oscillator and the target simulator and other circuitry rather than the EIO itself.

1. Introduction

A Microwave/ Millimeter Wave Dual Mode airborne missile simulator capability is going to be added to the present NRL Code 5740 simulator inventory.
The breadboard of the R.F. section of the mm wave radar for that Dual Mode is described in this preliminary report. It is unique in that it provides a coherent radar, using an incoherent R.F. transmitter.
It was decided to make the mm wave radar coherent in order to be able to simulate future threats even if these should use coherent radars. Furthermore, the radar could also be used for research in the mm wave range that requires a coherent radar. From the standpoint of the missile designer, using a radar emitting non - coherent pulses and still have the advantages of a coherent radar could be advantageous against ECM.

2. Basic description of the scheme.

The scheme of an IF Coherent Radar is not new. However, it appeared that the mm wave Extended Interaction Power Pulse Oscillator (EIO), due to its frequency stability, would work successfully with such a scheme. It is necessary that the phase within the r.f pulse is linear with time during the pulse, i.e., there is no chirp or random noise in the phase of the r. f. pulse. As our measurement shows, this is true to a large extent with the EIO we used in the setup described in this report.
The principle is this:
The r.f. phase in each r.f. pulse created by the r.f. pulse power oscillator is measured. The result is used to adjust the phase of a reference oscillator, such that when the signal

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arrives from the target, it will be demodulated by this adjusted reference signal in a coherent fashion. For example, assume that one particular r.f. pulse has a phase that leads the phase of the reference oscillator by 35 electrical degrees. Then 35 electrical degrees are added to the phase of the reference oscillator right after the pulse was transmitted. The phase shift in the ref. oscillator stays until the next rf pulse is transmitted.

Fig. 1 shows the basic IF Coherent scheme:

EIO 1 creates 94 GHz pulses of 1 kW peak power, 300 ns duration and 8 kHz repetition rate. The pulses are r.f. incoherent, i.e., each r.f. pulse starts with a phase that is randomly distributed between zero and 360 deg.. Modulator 2 keys the EIO with the repetition rate of pulse generator 3. The r.f. pulse created by the EIO is transmitted thru circulator 4 and antenna 5 to the target 6. The return from target 6 enters the antenna and is then fed to the receiver mixer 5 . Receiver mixer 5 receives its local oscillator signal from crystal controlled phase locked 93.86 GHz oscillator 17. The resulting I.F. constitutes incoherent pulses with 160 MHz center frequency. These are amplified in IF amplifier 7 and filtered in IF filter 8 in the conventional way.
Coherent Demodulator 9 provides the Doppler output; the other input to the demodulator is the COHO signal. This COHO signal is derived as follows:

The transmitted pulse leaks thru circulator 4 to receiver mixer 5. At the output of receiver mixer 5 then appears a 160 MHz Xmit pulse. This pulse is sent to phase discriminators 10 and 11, where it is compared with the 160 MHz signal from Reference Oscillator 12. Between the reference oscillator and the phase discriminators is 90 deg Hybrid 13, such that at the output of discriminators 10 and 11 appear voltages proportional to the sine and the cosine of the difference angle.
These voltages are fed to Sample & Hold circuits 14 and 15.
The sampling pulse is coinciding with the transmit pulse; it is derived from the Rep. Rate pulse generator 3.
The output voltages of S&H 14 and 15 represent the sine and the cosine of the phase difference between the r.f. pulses and the cw referenc oscillator 12.
These outputs are then fed to Phase Shifter 16, which adds the phase to the reference oscillator signal. Hence, the output of the Phase Shifter 16 is a 160 MHz signal with a phase that is adjusted to the phase of every transmitted r.f. pulse. Therefore, when the return pulse from the target arrives, it finds a COHO signal which has the proper phase for coherent demodulation.

3. The Test Setup

Fig. 2 shows the test setup block diagram. The path and the target are simulated by the Target Simulator Delay Repeater. It provides a 23 microsecond delay to simulate the return signal and a by - pass of the delay to provide the "leakage" of the Xmit pulse to the receiver mixer. The Doppler shift is simulated by insertion of pieces of 50 Ohm transmission line into the delay path with zero, lambda quarter and three quarter lambda electrical length.
Since the EIO had too much frequency drift during warm - up, (approx. 20 MHz), a frequency control loop was added to keep the center frequency of the EIO to 94 GHz +/-100kHz.
The dc/dc/ converters in the high voltage sources were synchronized with an integer multiple of the Repetition Rate in order to prevent spurious modulations of the r.f. by the dc/dc converter ripples.
Fig. 3 shows a photo of the bench setup.

4. Results

4.1 Discussion of signals

Fig. 4 shows an oscillogram of the phase discriminator output . I output, which is proportional to sin(phi) is deflecting horizontally, Q output (proportional to cos(phi)) is deflecting vertically. Phi is the difference between the phase of the r.f. pulses of the E.I.O and the reference oscillator. The result is a circle, as should be.
Fig. 5 shows the output of the Phase Shifter with 50 kHz test signals at inputs I and Q. The signal at I leads that on Q by 90 degrees. The rf input was 160 MHz. Shown is the spectrum of the output signal at 160 MHz. Since the "Phase Shifter" is functionally the same as a Single Sideband Modulator, Fig. 5 shows the "carrier" down 33 dB and the suppressed (lower) "sideband" down 30 dB. In order to better designate its function, the Phase Shifter was not called a SSB modulator.

Fig. 6, 7 and 8 show the output of the signal pulse behind the Coherent Demodulator. In order to demonstrate the Doppler shift, zero, lambda quarter and 3/4 lambda long delay lines were added in the signal path, resulting in positive peak, zero and negative peak pulse output.

4.2 Signal to Clutter Ratio

The signal to clutter ratio of the signal output behind the coherent demodulator was measured by feeding the pulse to a Sample and Hold circuit. The clutter ratio CL is the ratio between the average peak amplitude of the pulse and the r.m.s of

the variation from that average. A true rms voltmeter was used to measure the variation, and a d.c. voltmeter to measure the average peak. The ratio measured was CL = 26 dB.

The delay was then adjusted to obtain zero average pulse output as in fig. 7. The ratio of average peak for max. output to the r.m.s deviation from zero average was 16 dB.

The clutter ratio of the E.I.O itself is probably better than 26 dB, because this was close to the limitation of the test set-up itself, primarily caused by the residual phase noise of the 94.3 and 93.84 GHz local oscillators and the accuracy of the phase adjustment circuits. This was verified by injecting a 300 MHz pulse derived from a HP 608 signal generator into the Target Simulator (see fig. 2) in lieu of the EIO derived transmit pulse. The clutter ratio measured for that case was 29 dB.

5. Description of the circuits

5.1. The E.I.O.

The E.I.O (Extended Interaction Oscillator) was the type VKB 2445S2 by Varian Canada. Its pulse output power is approx. 1 kW @ 94 GHz. It is keyed by a 3 kV pulse at the grid; its operational dc voltage on the cathode is -20 kV, the grid-cathode bias is -3 kV.

5.2 The HV modulator for the E.I.O. grid

Fig. 9 shows the schematic for the modulator. The drive pulse is fed to the cathode of the E.I.O. rather than the grid. Driving the grid instead does not considerably reduce the drive current requirement due to grid/cathode capacity, whereas driving the cathode permits elimination of the HV pulse transformer. In this scheme, the grid voltage is constant at -20kV, and during the pulse the cathode is driven negative by 3 kV from -17 kV to -20 kV by keying tube Q2 (8847A) on. Q2 and the transformer providing the 3 kV EIO grid bias, the EIO heater voltage and d.c. supply voltages for the grid of the driver tube and the pre-driver FET amplifier are located in an oil bath, further the H.V. capacitors.

Fig. 10 shows the high voltage d.c supplies, -17 kV for the cathode of the E.I.O. and 3.7 kV for the plate of the driver tube. The d.c. to HV converters are commercially available from Advanced HV Co.. Fig. 11 shows the driver circuitry of those converters by Advanced HV Co., with a custom synchronization circuit added by NRL. As mentioned above, the d.c. converters

were synchronized with a harmonic of the radar's repetition frequency in order to prevent ripple-induced jitter in the r.f. phase of the EIO. Further, Also, an input controlling the high voltage for tuning control of the E.I.O. was added. The tuning sensitivity was approx. 50 kHz /V . The input signal for this AFC is coming from the pulse r.f. discriminator, see fig. 2 and fig. 21.
Fig. 12 shows the connections of the EIO modulator.

5.3 The Phase Locked Local Oscillator (PLLO)

Fig. 13 shows the block diagram of the PLLO.
Gunn oscillator 4 provides a 93.84 GHz output.
A sample of this is mixed in Harmonic Mixer 6 with the tenth harmonic of 9.362 GHz source 7, resulting in a 220 MHz I.F..
The 9.362 GHZ crystal controlled source 7 is commercially available from TCI, model # M5020 - 9362.
The I.F. is amplified by amplifier 8 and mixed with the 220 MHZ signal from crystal oscillator 10 in phase discriminator 9.
The output of phase discriminator 9 controls the d.c. output of GUNN d.c. supply 3 via FET switch 13. Since the frequency of the GUNN oscillator depends on the d.c. supply level (typically 200 ... 300 MHz/V), the phase lock loop is closed.
The output from phase discriminator 9 is also sent to lock detector 12 thru low pass filter 11. Low pass filter 11 suppresses the 220 MHz leakage from phase discriminator 9.
GUNN Heater Control 16 keeps the GUNN oscillator at a temperature of 45 deg. C.
Lockup procedure:
After turn-on, switch 13 is open, opening the phase lock loop, until the Gunn oscillator reaches its proper temperature. This way, lockup to any wrong frequency during warm-up is prevented.
Switch 2 is closed, feeding the signal from Saw Tooth Generator 1 to GUNN d.c. supply 3, therby sweeping the GUNN oscillator by approx. 100 MHz at a rate of about once per second.
GUNN Heater Control 16 senses when the GUNN oscillator has reached its proper temperature and closes switch 13, thereby closing the phase lock loop. Lock detector 12 senses when lock condition occurs and opens switch 2, thus interrupting the sweep. Should phase lock be lost, Lock Detector 12 closes switch 2 again, thereby restarting the sweep.
The condition of switch 13 closed and switch 2 open is sensed by logic 14, signalling lock condition by lighting LED 15.
Isolator 5 separates the GUNN oscillator from the load.

Fig. 14 shows the schematic of the PLLO, fig. 15 its printed circuit board layout and fig. 16 the p.c. board mask.

5.3.1 Measurement of Noise Spectrum of PLLO

Since no source with better spectral purity was available, two almost identical such crystal controlled P.L.L. oscillators were mixed down to 460 MHZ. Fig. 17 shows the resulting spectrum with 1 kHz resolution and fig. 18 with 100 kHz resolution. At 10 kHz off carrier, fig. 17 shows the noise to be 40 dB below carrier, corresponding to 70 dB in 1 Hz bandwidth. Assuming equal contributions of noise from each oscillator, its noise level is 73 dB below carrier in 1 Hz bandwidth. Integrated in a 3 MHz bandwidth, using fig. 17 and 18 for the graphical integration, the total noise is 29 dB below carrier.

5.4 Timing and Control Circuit

Fig. 19 shows the Timing and Control Circuit. It provides the transmit drive pulse, the receiver blanking pulse, the drive signals for the receiver protection switches and the receiver protection electronics and the transmitter VSWR detector and interlock.

5.5 Phase Measuring and Shifting Circuit, see fig.20, schematic.

The 160 MHZ I.F. transmitter leakage pulse enters at point A. It is fed to a 90 deg. hybrid, whose two outputs feed two phase discriminators. The other input B of the phase discriminator comes from the 160 MHz reference oscillator; in the case of this bench setup, an HP 608D signal generator was used.
The outputs of the phase discriminators are entered into two fast Sample and Hold circuits; the sample pulse is derived from the transmit trigger pulse via monostable pulse generators 74LS123. Two 560 pF capacitors provide the "hold" function. Voltage droop during the repetition interval across these capacitors is a problem; a better solution would be a combination of an A to D converter with a S & H input, followed by a D/A converter. This would eliminate the droop and increase accuracy. Moreover, in a further improvement, the D/A converter and the Phase Shifter could be eliminated and the phase shift could be performed digitally in the Radar Data Processor Computer. The droop in the present design was quite small, none was visible on the scope. The sample function is performed by two FET's; one charges the holding capacitor during the transmit pulse, the other discharges it at the end of the repetition interval.
The I and Q signals appear at the output of the S&H circuit (points 1 and 2). These signals are fed into the Phase Shifter, consisting of two balanced mixers, which together with two operational amplifiers form four quadrant multipliers. The other input to the mixers is the 160 MHZ reference signal B;

it is the same as the one mentioned above, just with a different level.Between the input of this ref. signal and the mixers is a 90 deg. hybrid, providing the necessary 90 degrees out of phase signal. Low pass filters at the output of the mixers eliminate higher harmonics of the 160 MHz signal; the outputs are then combined in a simple adder. The output D of this adder is the COHO signal used for coherent demodulation.

5.6 Coherent Demodulator

As coherent demodulator (see fig. 2) was used a MINICIRCUIT SBL-1 balanced modulator.

5.7 EIO Frequency Control

Fig. 21 shows the pulse r.f. frequency discriminator for the EIO AFC.

5.8 Measurement of Peak to Clutter Ratio of coherently demodulated signal pulse

As mentioned above, the peak to clutter ratio of the coherently demodulated pulse was measured by using a Sample and Hold circuit. The sampling signal was derived using a 100A Datapulse pulse generator, which was triggered by the transmit pulse and had a delay of 23 microseconds to match the delay in the repeater simulating the signal path (see fig. 2). Fig. 22 shows the S&H circuit used for the measurement.

FIGURE CAPTIONS

Fig. 1: Coherent MM Wave Radar with Incoherent Transmitter, Block Diagram

Fig. 2: Coherent MM Wave Radar with Incoherent Transmitter, Block Diagram of Test Setup

Fig. 3: Breadboard of Test Setup

Fig. 4: Phase Discriminator Output

Fig. 5: Performance of Phase Shifter

Fig. 6: Output of Coherent Modulator

Fig. 7: Output of Coherent Modulator

Fig. 8: Output of Coherent Modulator

Fig. 9: Schematic of EIO Modulator

Fig. 10: High Voltage DC Supplies

Fig. 11: HV Supply by Advanced HV Corp. with Circuits Added by NRL

Fig. 12: HV Modulator Connections

Fig. 13: Receiver Phase Locked Local Oscillator (PLLO) Block Diagram

Fig. 14: Receiver PLLO Schematic

Fig. 15: PLLO Printed Circuit Board Layout

Fig. 16: P.C. Board Mask for PLLO

Fig. 17: Spectrum of PLLO, Mixing Down to 460 MHz with Second PLLO

Fig. 18: Same as Fig. 14 but with Different Resolution

Fig. 19: Radar Timing and Control Circuits

Fig. 20: Phase Measuring and Phase Shifting Circuit Schematic

Fig. 21: Schematic of Pulse R.F. Discriminator for EIO AFC

Fig. 22: Sample and Hold Circuit for Peak to Clutter Measurement

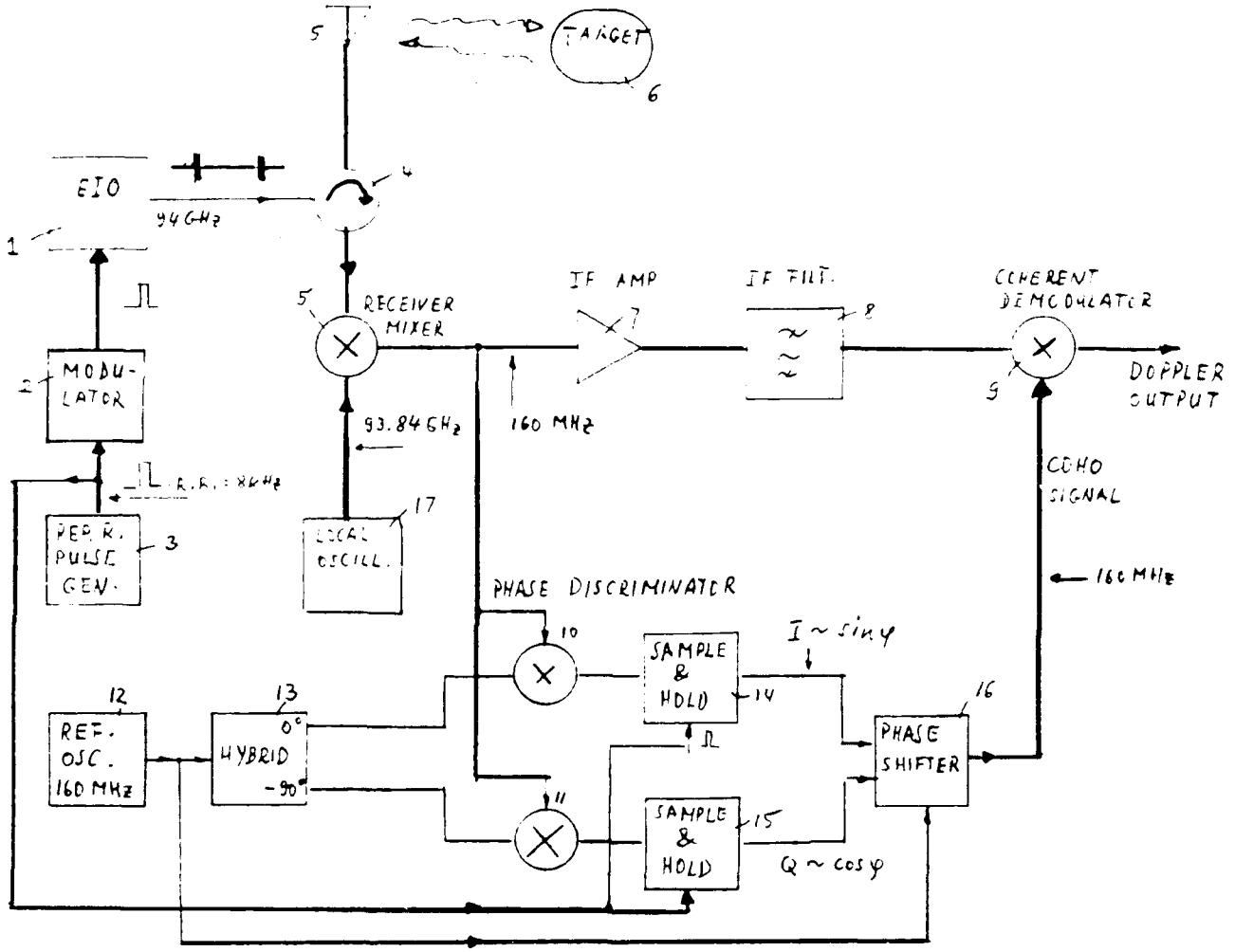


Fig. 1 — Coherent MM Wave Radar with Incoherent Transmitter

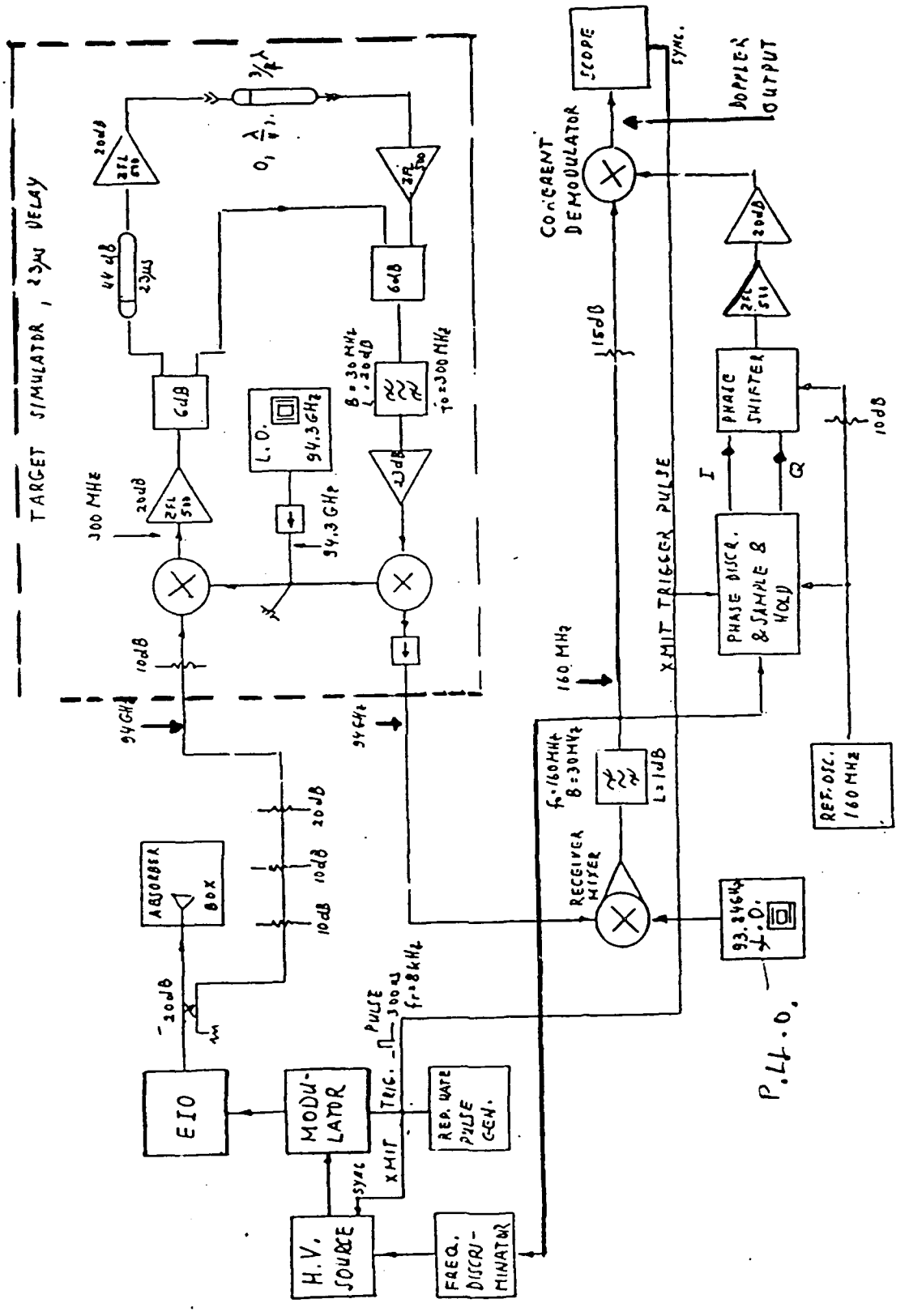


Fig. 2 — Coherent MM Wave Radar with Incoherent Transmitter Test Setup

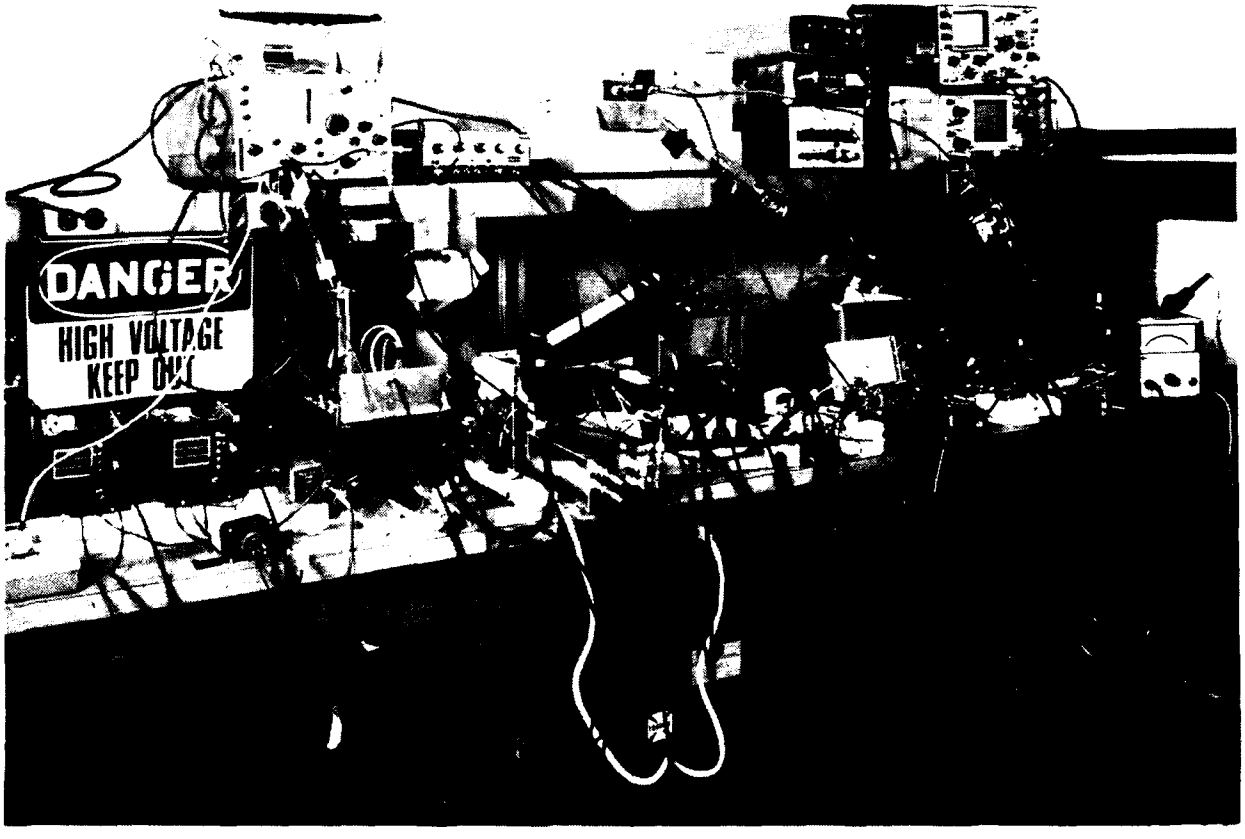


Fig. 3 -- Breadboard of Test Setup

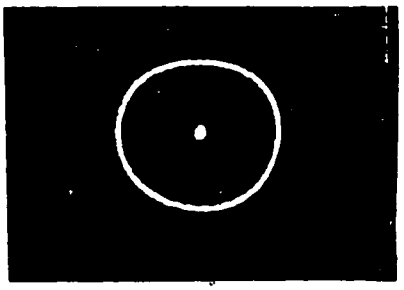


Fig. 4 -- Phase Discriminator Output

I is on X - Axis
Q is on Y - Axis

Hor: 1 V/Div.
Vert.: 1 V/Div.

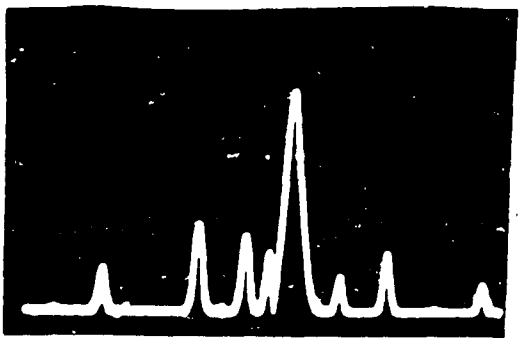


Fig. 5 — Testing the Phase Shifter

Input:	Two 50 kHz signals with 90 deg. phase shift to I and Q. I leads Q.
and	160 MHz c.w.
Output:	Spectrum of 160 MHz signal
Hor.:	100 kHz/Div.
Vert.:	10 dB/Div.

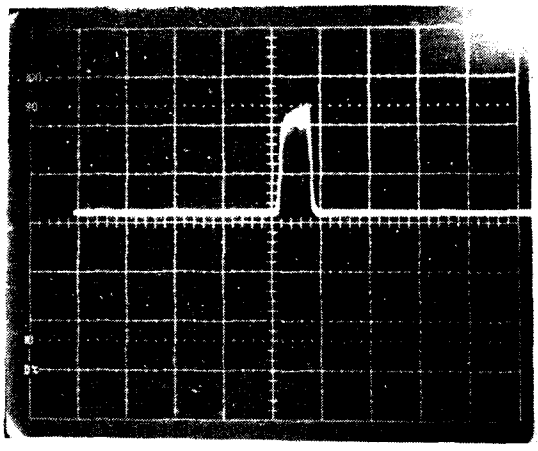


Fig. 6 — Output of Coherent Demodulator Signal Pulse has 23 μs Delay

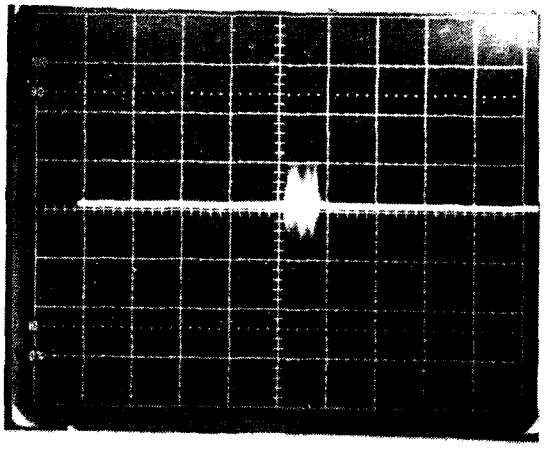


Fig. 7 — As Fig. 6, but with $\lambda/4$ delay added

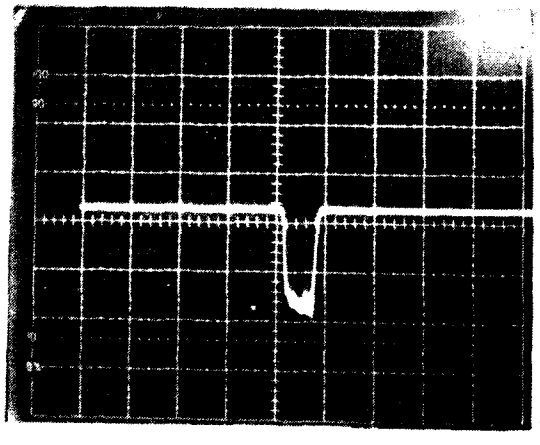


Fig. 8 — As Fig. 6, but with 3/4 λ delay added

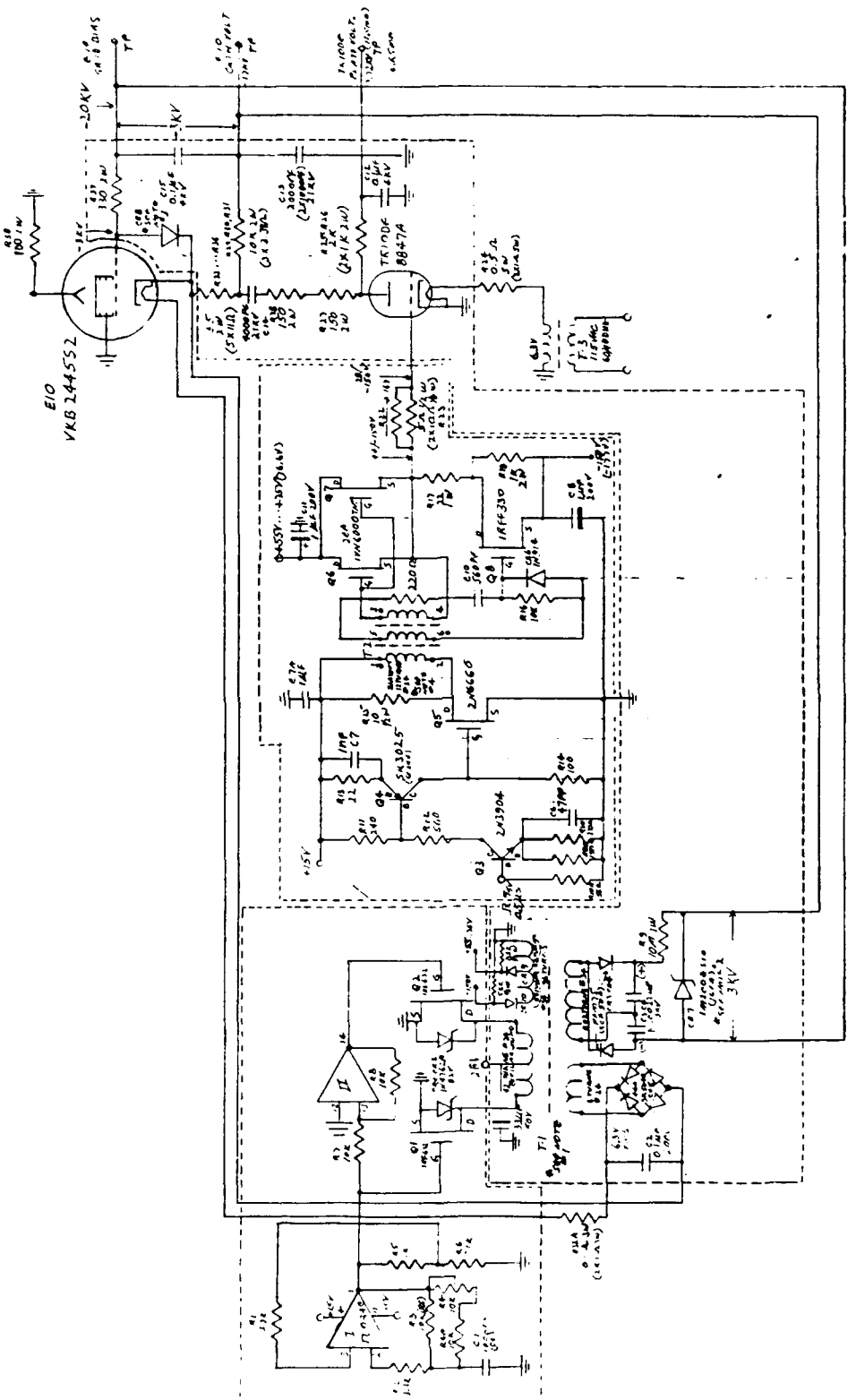


Fig. 9 — Schematic of EIO Modulator

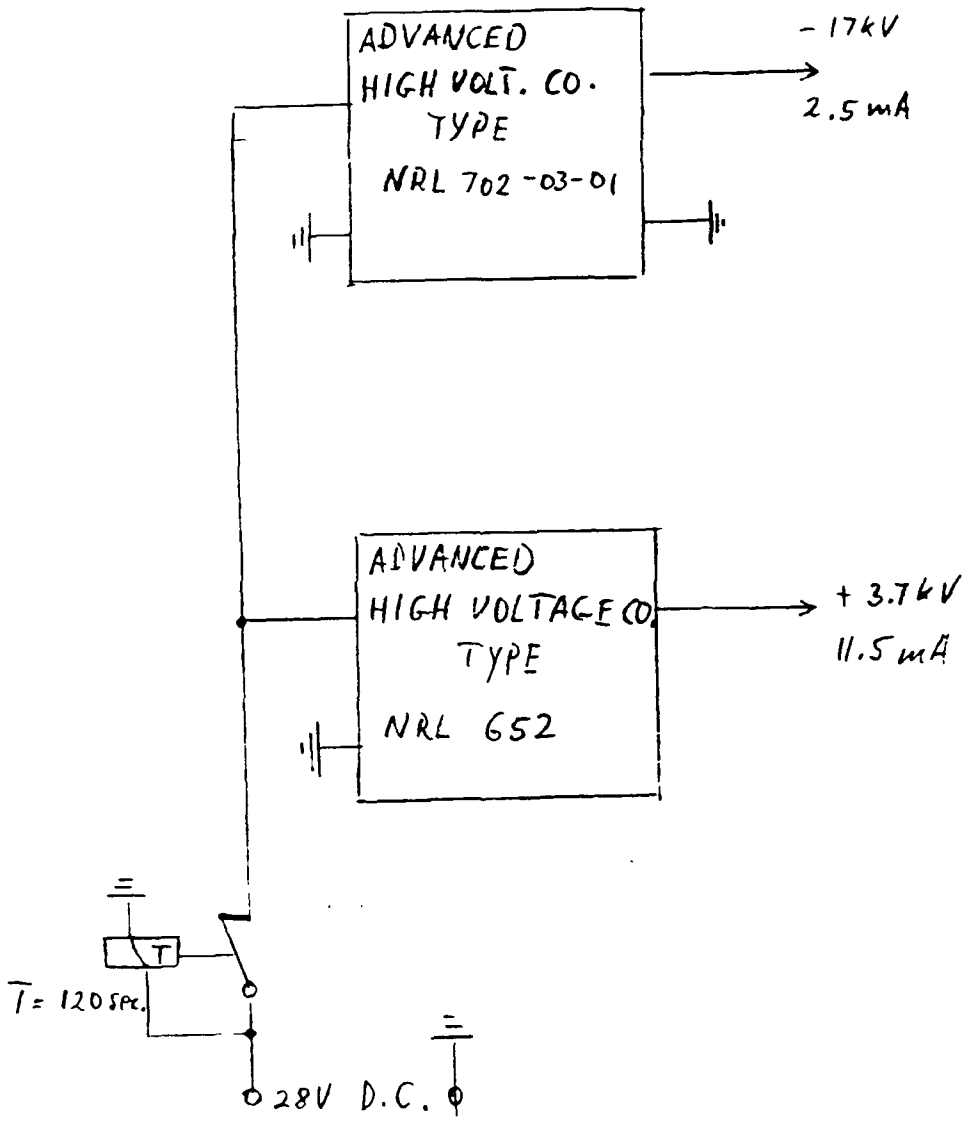


Fig. 10 — High Voltage D.C. Supplies

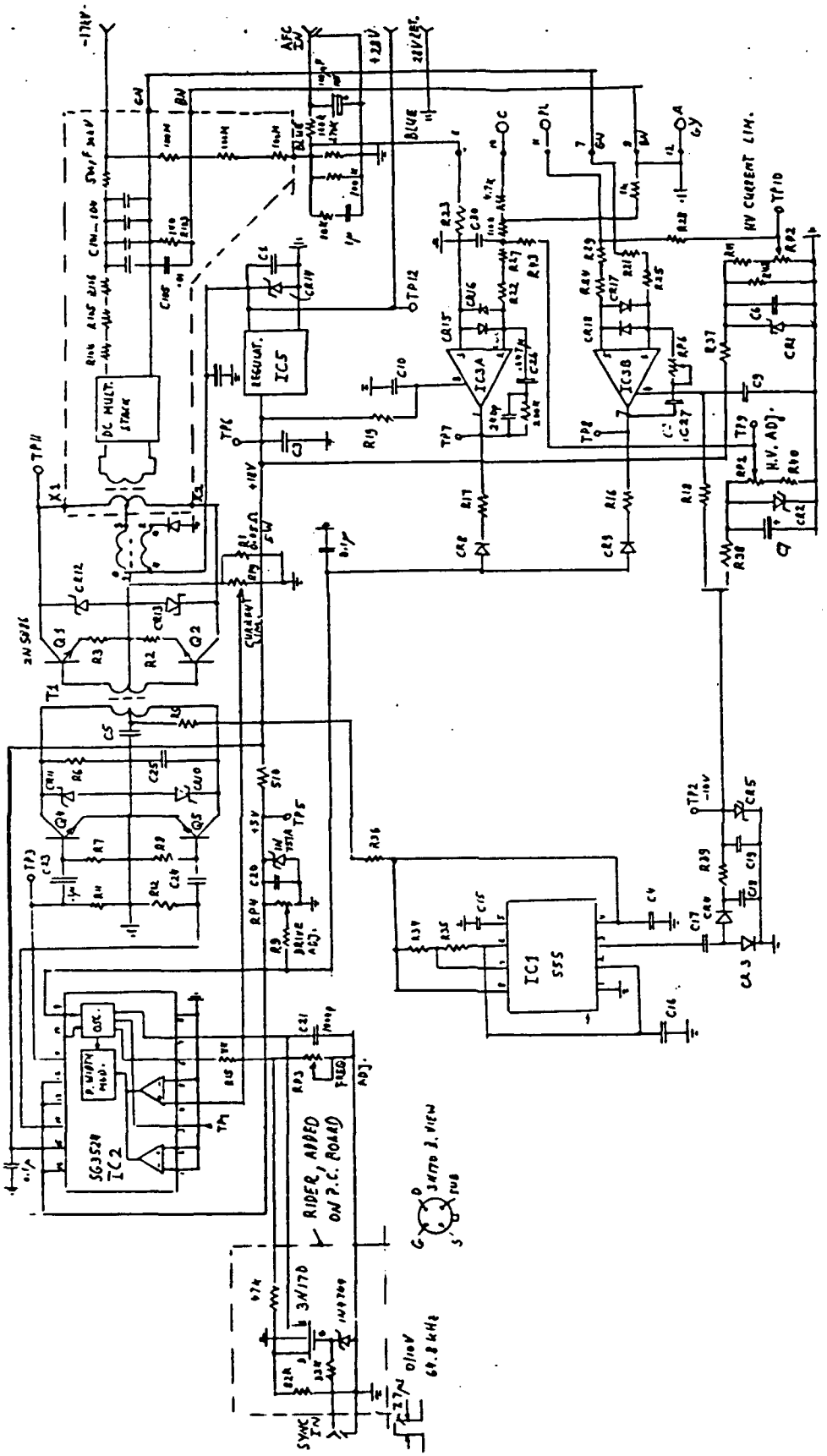


Fig. 11 — -17 kV HV Supply by Advanced High Voltage Corp. with Sync Circuit and AFC Input Added

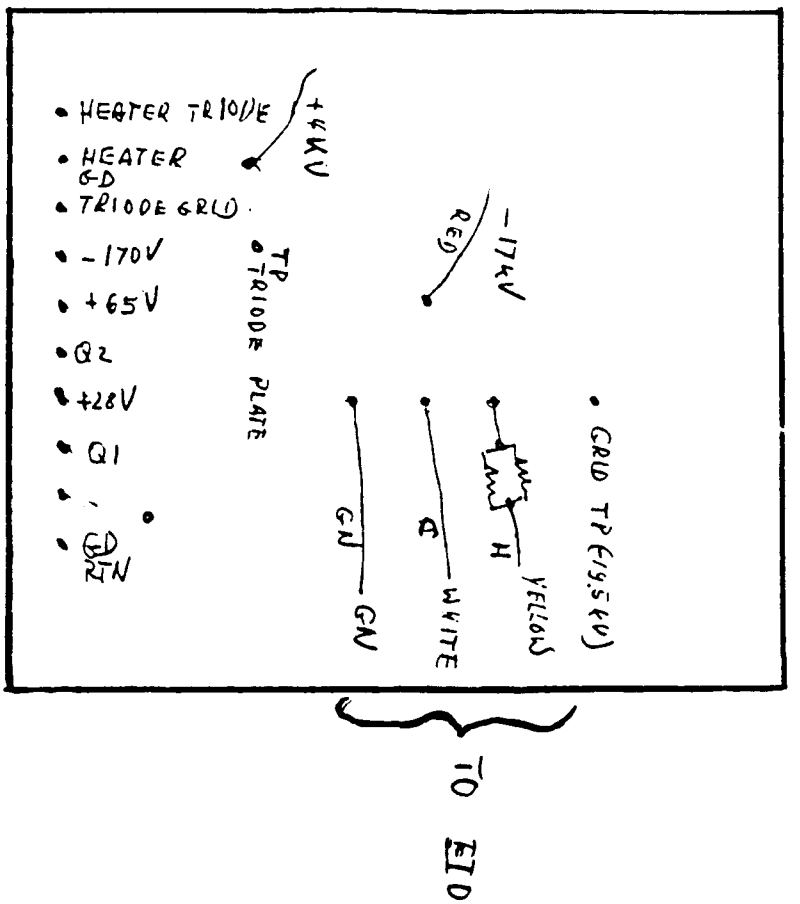


Fig. 12 — HV Modulator Connections

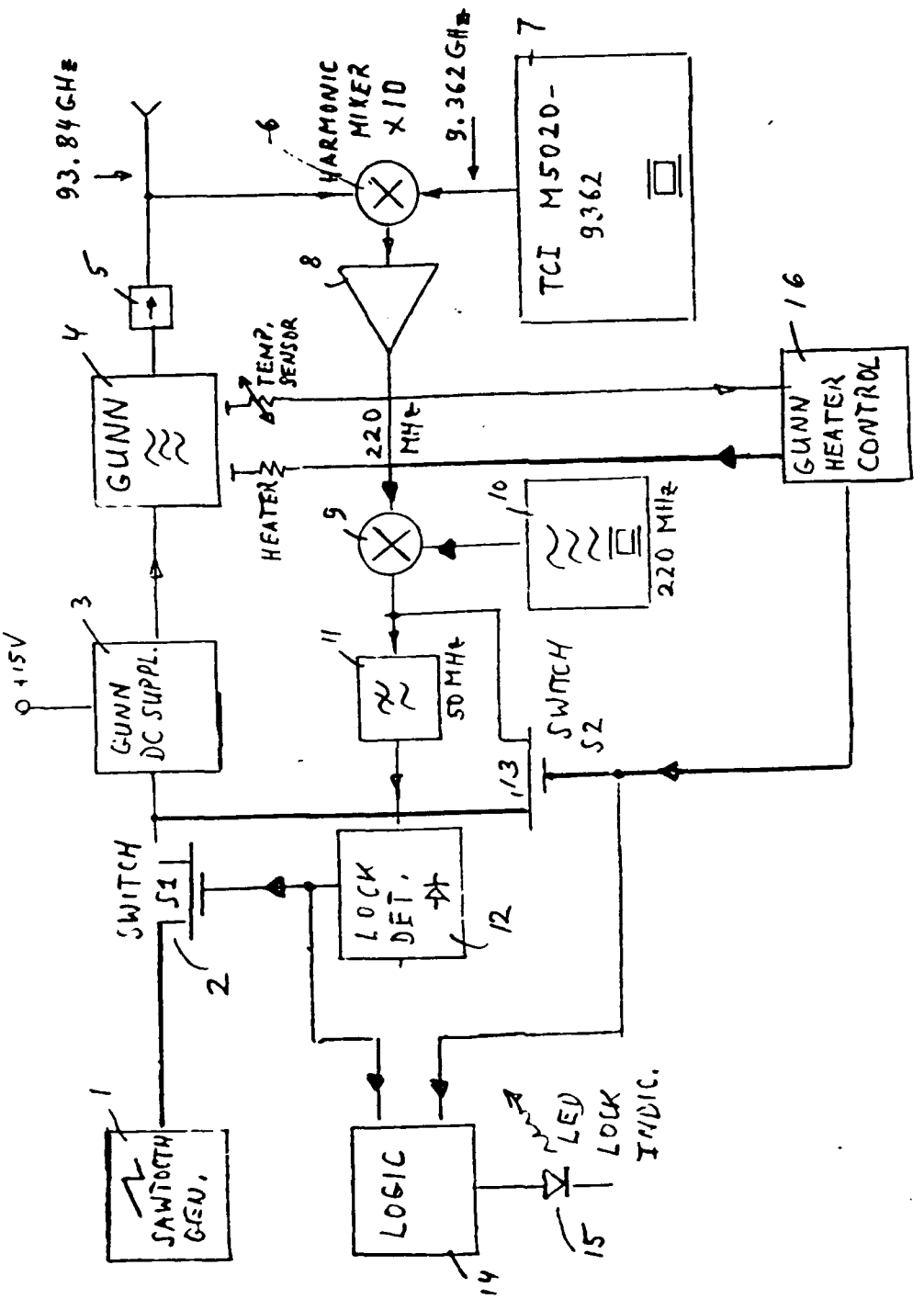


Fig. 13 — Block Diagram of PLLO

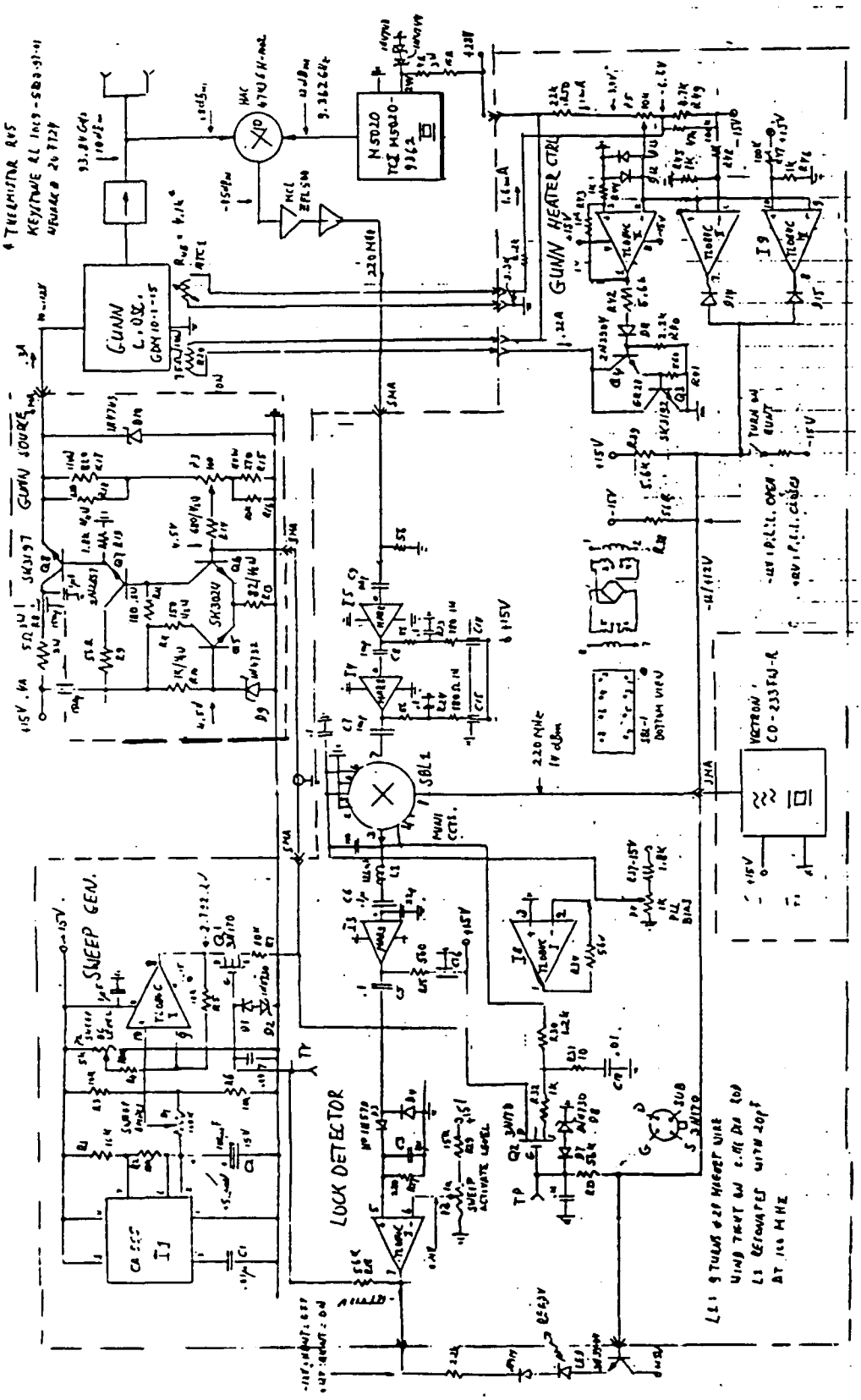


Fig. 14 — Phase Lock for GUNN Oscillator for Dual Mode Radar

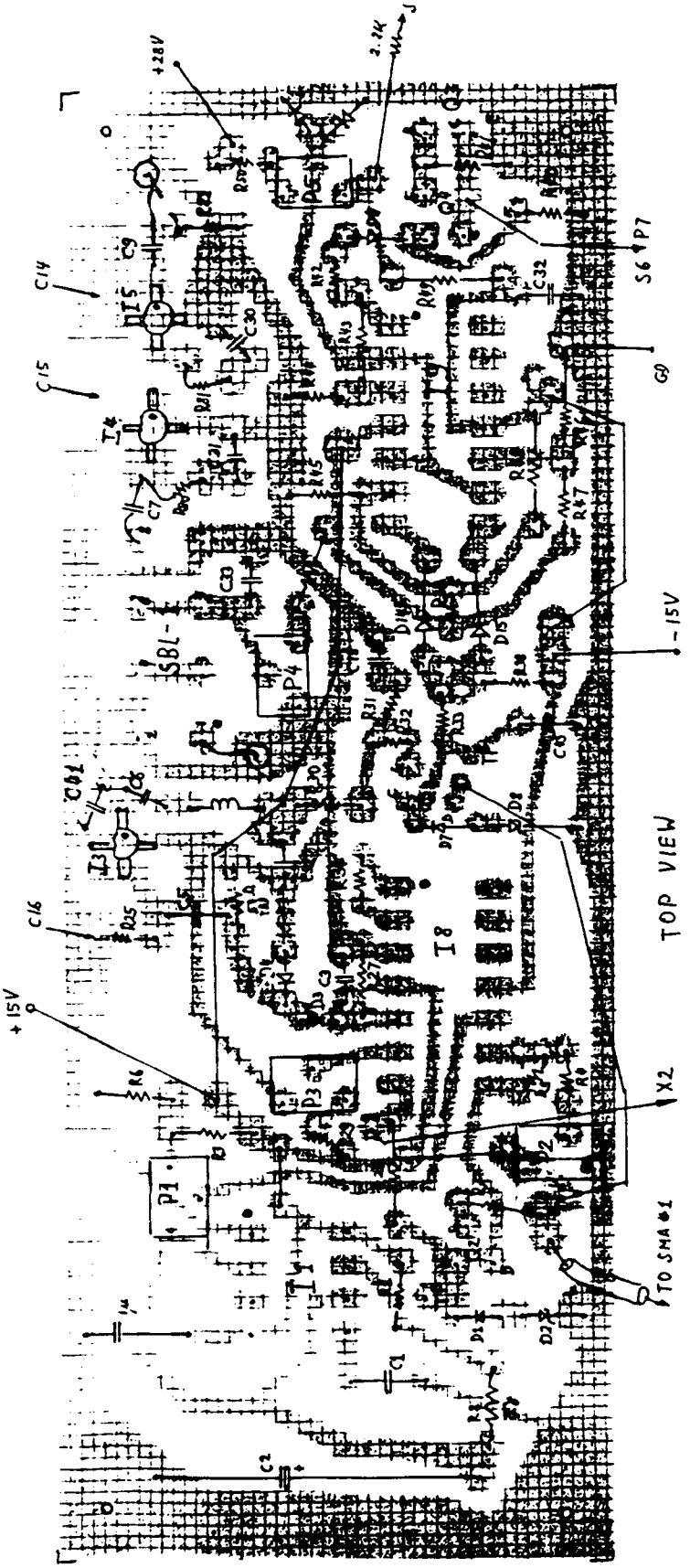


Fig. 15 — P.C. Board Layout

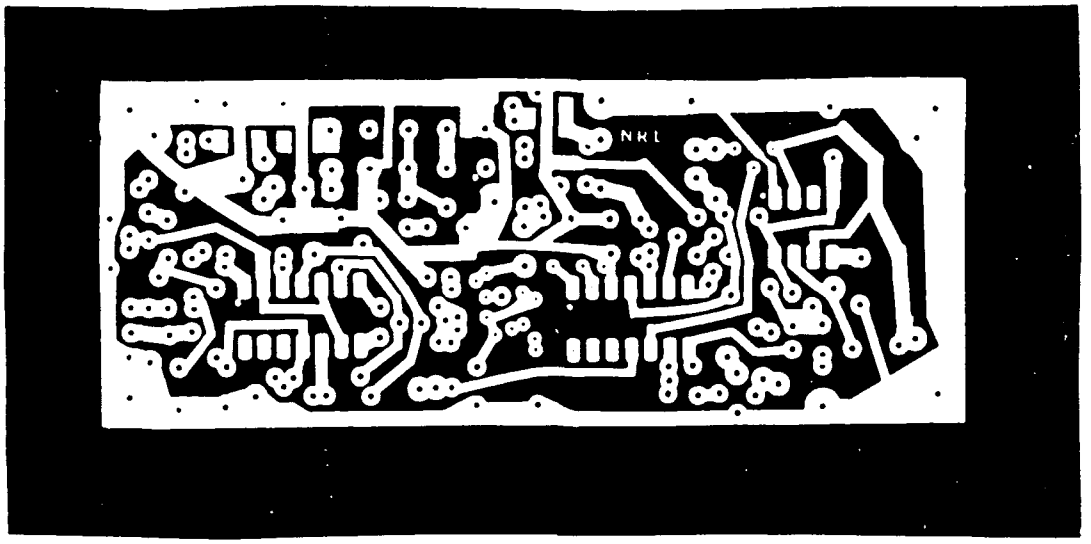


Fig. 16 — P.C. Board Mask for PLLO

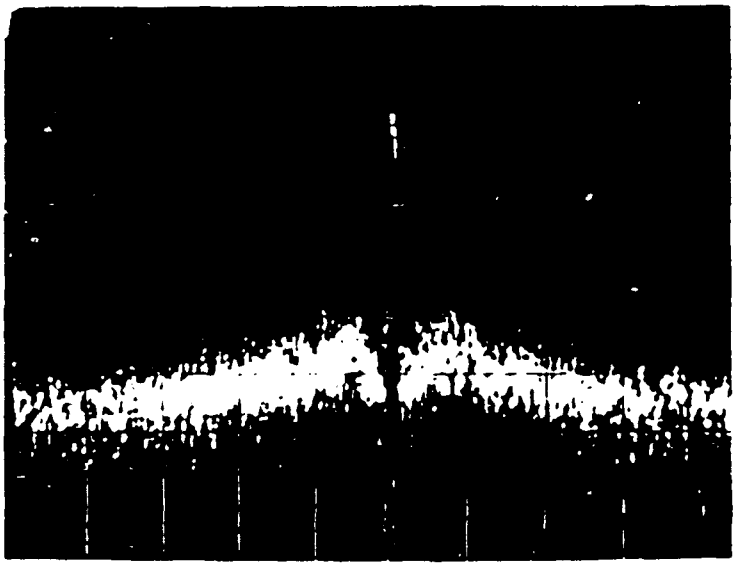


Fig. 17 — Spectrum for Two Crystal Controlled Phase Locked GUNN Oscillator Mixed Down to 460 MHz

Vert.: 10 dB/div.
Hor.: 30 kHz/div.
Resol. B.W. 1 kHz

Fig. 18 — Same as Fig. 17
Except Hor. = 3 MHz/div.
Resol. B.W. = 100 kHz

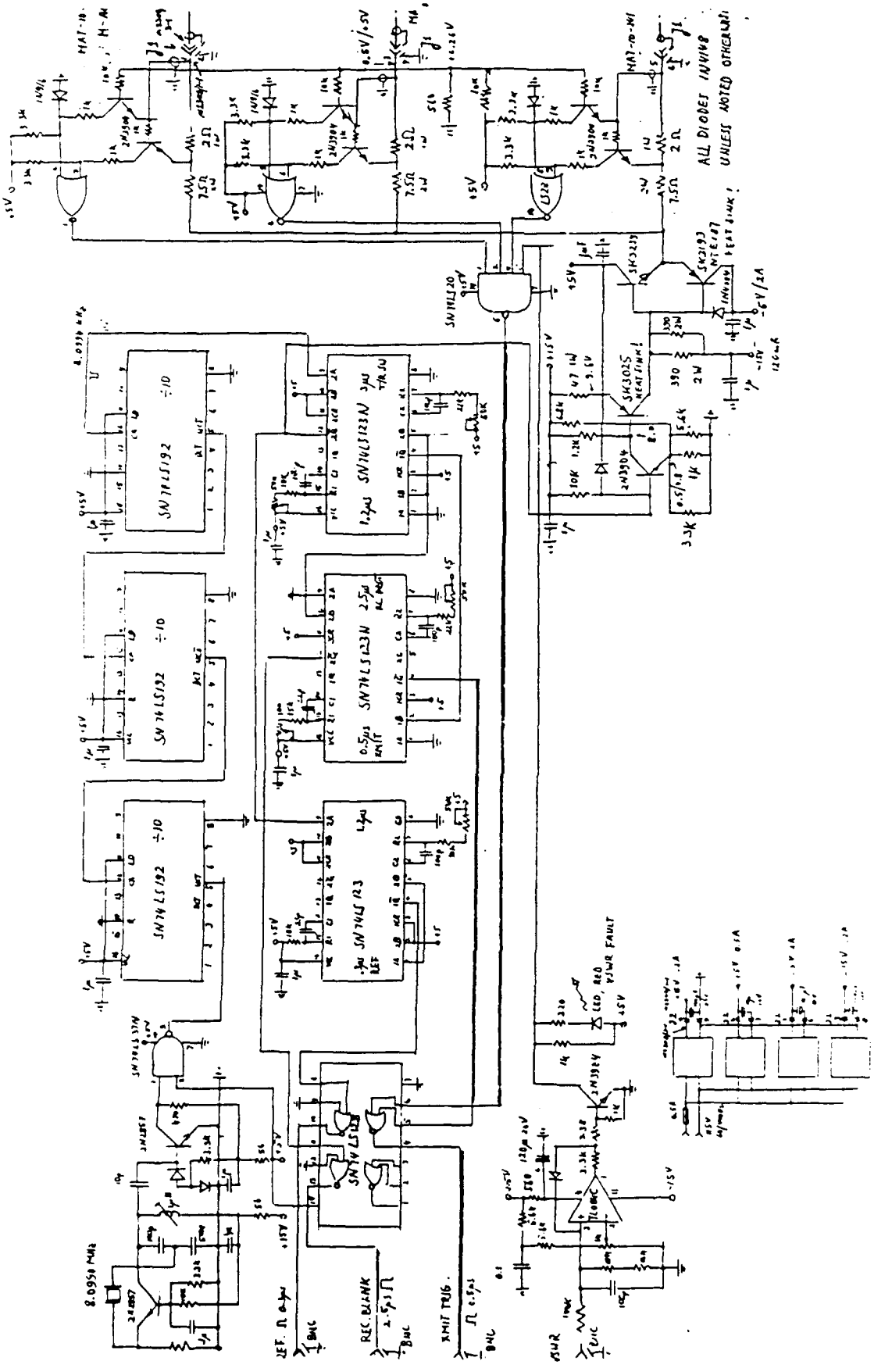


Fig. 19 — Radar Control and Timing Circuit Dual Mode Radar

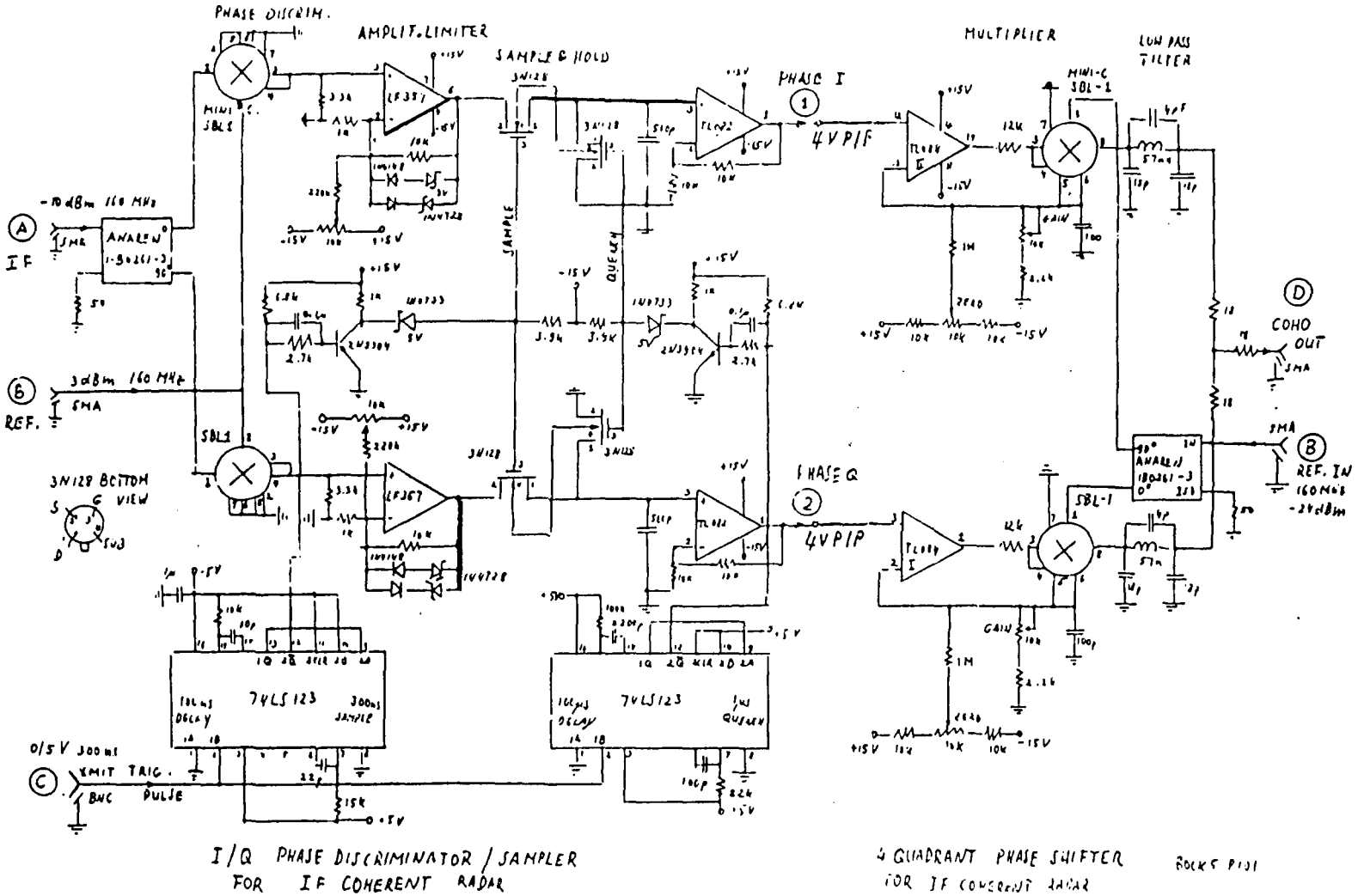
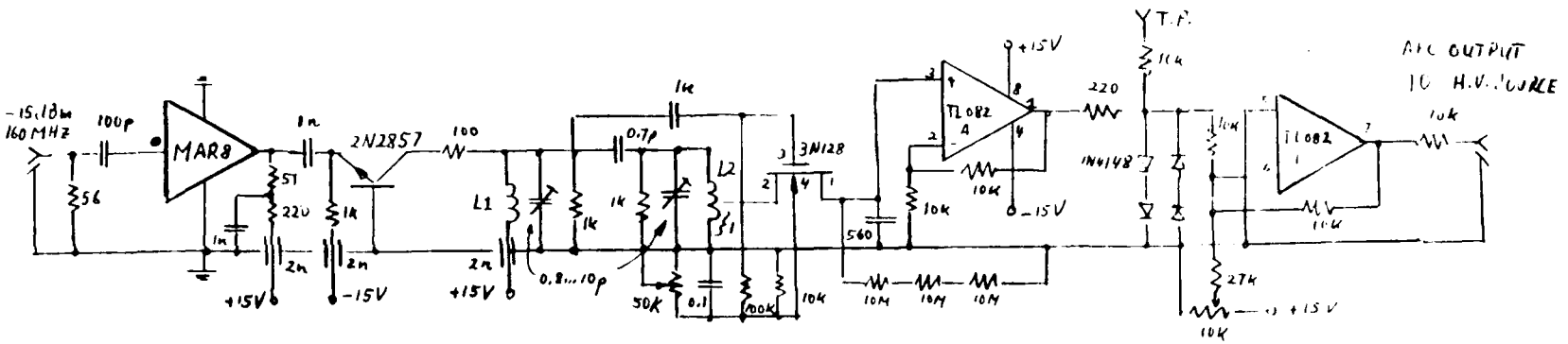


Fig. 20 — Phase Measuring and Phase Shifting Circuit Schematic



L1 : 4 TURNS ON 1/4" DIA ROD, # 16 MAGNET WIRE

L2 : 4 TURNS ON 1/4" DIA ROD, # 16 MAGNET WIRE, TAP AT 1 TURN . COILS RESONATE AT 160MHz W. 10 pF

Fig. 21 — RF Pulse Frequency Discriminator

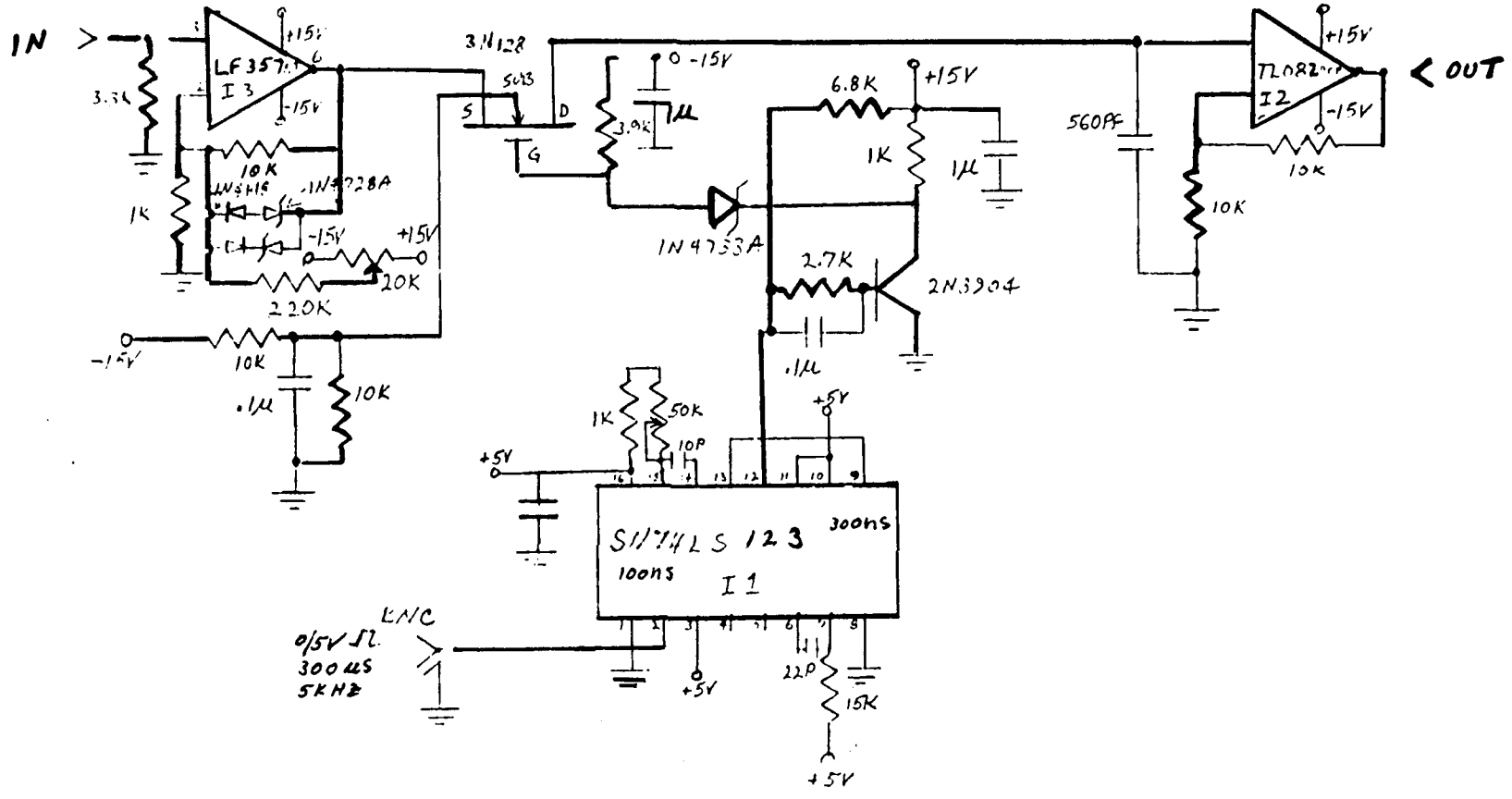


Fig. 22 — Sample and Hold Circuit for Peak to Clutter Measurement

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